

09/09/372

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L34	0	(first clock circuit AND second clock circuit AND phase detector AND error signal AND synchronization control circuit AND clock distribution circuit).clm.	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/12/09 18:59
L35	0	(first clock circuit AND second clock circuit AND phase detector AND error signal AND synchronization control circuit AND clock distribution circuit AND loop filter circuit AND oscillator AND pulse generator AND arbiter circuit AND amplifier circuit).clm.	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/12/09 18:59

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	8	generat\$3 and (first clock signal\$1 same first error signal\$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 14:57
L2	8	generat\$3 and (second clock signal\$1 same first error signal\$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 14:57
L3	0	generat\$3 and (first error signal\$1 same (phase different same (first clock near5 second clock)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 14:59
L4	69	phase detector\$1 same first error signal\$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:45
L5	1	I4 and (I1 and I2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 15:00
L6	2	I4 and (I1 or I2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 17:05
L7	7	I1 and I2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:26
L8	36934	phase detector	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 17:06

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L9	4	I7 and I8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 17:07
L10	348	generat\$3 and (error signal\$1 same different phase)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 17:07
L11	0	I9 and I10	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 17:07
L12	21306	327/47 or 713/500 or 713/501 or 713/503 or 713/400 o or 714/798 or 714/707 or 714/699 or 714/700 or 714/731 or 714/744 or 714/814 or 714/? or 327/? or 713/? or 702/?	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:29
L13	89	I8 and I10	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:29
L14	2	I12 and I13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:34
L15	4	I4 and I13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:35
L16	7	I1 and I2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:35

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L17	1	I16 and I4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:36
L18	4	I16 and I8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:36
L19	4	I18 and (I15 or I16)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:36
L20	3	I12 and I19	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:43
L21	7124	generat\$3 same clock signal\$1 same integrated circuit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:43
L22	1407	synchroniz\$3 and (phase\$1 same clock signal\$1 same error signal\$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:44
L23	88	I21 and I22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:44
L24	57	I23 and I8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:45

EAST Search History

L25	0	I24 and I10	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:45
L26	1	I24 and I4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:45
L27	4564	phase detector\$1 same error signal\$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:45
L28	46	I24 and I27	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:45
L29	146	first clock signal\$1 same error signal\$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:46
L30	113	second clock signal\$1 same error signal\$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:46
L31	88	I29 and I30	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:46
L32	7	I31 and I28	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:57

EAST Search History

L33	2	I32 and I12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/12/09 18:47
L34	0	(first clock circuit AND second clock circuit AND phase detector AND error signal AND synchronization control circuit AND clock distribution circuit).clm.	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/12/09 18:59
L35	0	(first clock circuit AND second clock circuit AND phase detector AND error signal AND synchronization control circuit AND clock distribution circuit AND loop filter circuit AND oscillator AND pulse generator AND arbiter circuit AND amplifier circuit).clm.	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/12/09 18:59